MH255 Hall-effect sensor is a temperature stable, stress-resistant, Low Tolerance of Sensitivity micro-power switch. Superior high-temperature performance is made possible through a dynamic offset cancellation that utilizes chopper-stabilization. This method reduces the offset voltage normally caused by device over molding, temperature dependencies, and thermal stress.

MH255 is special made for low operation voltage, 1.7V, to active the chip which is includes the following on a single silicon chip: voltage regulator, Hall voltage generator, small-signal amplifier, chopper stabilization, Schmitt trigger, CMOS output driver. Advanced CMOS wafer fabrication processing is used to take advantage of low-voltage requirements, component matching, very low input-offset errors, and small component geometries. This device requires the presence of omni-polar magnetic fields for operation.

The package type is in a Halogen Free version has been verified by third party Lab.

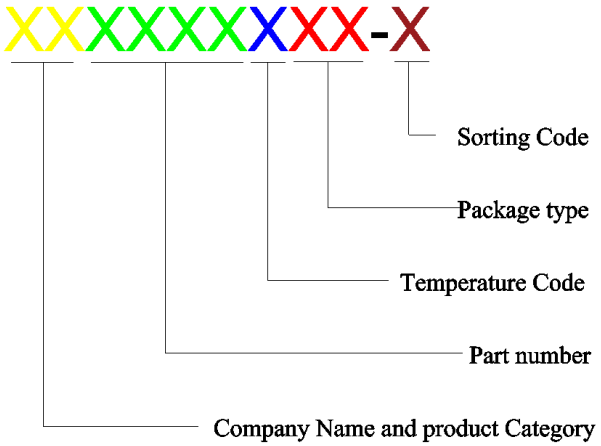
Features and Benefits

- CMOS Hall IC Technology
- Strong RF noise protection
- 1.7 to 5.5V for battery-powered applications
- Omni polar, output switches with absolute value of North or South pole from magnet
- Operation down to 1.7V,Micro power consumption
- High Sensitivity for reed switch replacement applications
- Multi Small Size option
- Low sensitivity drift in crossing of Temp. range
- Ultra Low power consumption at 5uA (Avg)
- High ESD Protection, HBM>±4KV(min)
- Totem-pole output
- RoHS compliant 2011/65/EU and Halogen Free.

Applications

- Solid state switch
- Handheld Wireless Handset Awake Switch (Flip Cell/PHS Phone/Note Book/Flip Video Set)
- Lid close sensor for battery powered devices
- Magnet proximity sensor for reed switch replacement in low duty cycle applications
- Water Meter
- Floating Meter
- PDVD
- NB

Ordering Information



Company Name and Product Category

MH:MST Hall Effect/MP:MST Power IC

Part number

181,182,183,184,185,248,249,276,477,381,381F,381R,382…..

If part # is just 3 digits, the forth digit will be omitted.

Temperature range

E: 85 ℃, I: 105 ℃, K: 125 ℃, L: 150 ℃

Package type

UA:TO-92S,VK:TO-92S(4pin),VF:TO-92S(5pin),SO:SOT-23,

SQ:QFN-3,ST:TSOT-23,SN:SOT-553,SF:SOT-89(5pin),

SS:TSOT-26,SD:DFN-6

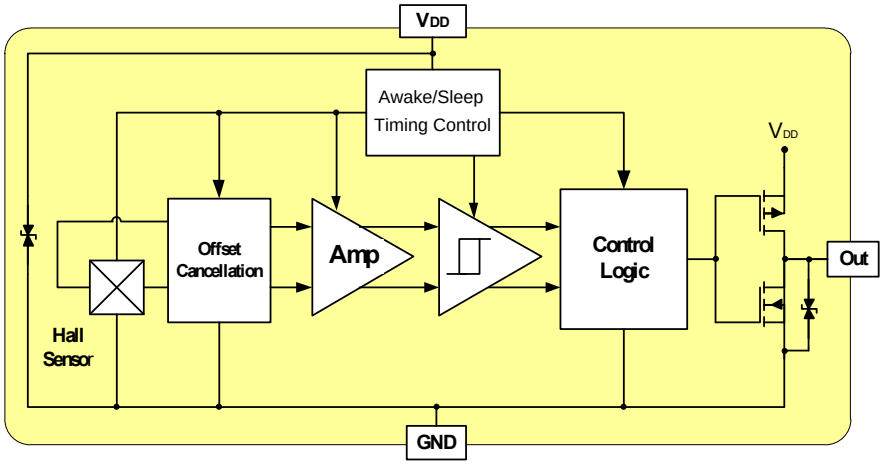
Sorting

α,β,Blank…..

Part No.	Temperature Suffix	Package Type
MH255ESO	E(-40℃ to +85℃)	SO(SOT-23)
MH255EST	E(-40℃ to +85℃)	ST (TSOT-23)
MH255ESP	E(-40℃ to +85℃)	SP (PSOT-23)
MH255EUA	E(-40℃ to +85℃)	UA (TO-92S)
MH255ESN	E(-40℃ to +85℃)	SN (SOT-553)
MH255ESQ	E (-40℃ to + 85℃)	SQ (SQ2020-3)

Custom sensitivity selection is available by MST sorting technology

Functional Diagram



***Note**: Static sensitive device; please observe ESD precautions. Reverse V_{DD} protection is not included. For reverse voltage protection, a 100Ω resistor in series with V_{DD} is recommended.*

MH 255, HBM>±4KV which is verified by third party lab.

Absolute Maximum Ratings *At(Ta=25℃)*

Characteristics		Values	Unit
Supply voltage,(V_{DD})		7	V
Output Voltage,(V_{out})		7	V
Reverse Voltage , (V_{DD}) (V_{OUT})		-0.3	V
Magnetic flux density		Unlimited	Gauss
Output current,(I_{OUT})		1	mA
Operating temperature range, (Ta)		-40 to +85	℃
Storage temperature range, (Ts)		-65 to +150	℃
Maximum Junction Temp,(Tj)		150	℃
Thermal Resistance	(θ_{JA})ST / SN / UA / SP / SQ	310/540/206/625/540	℃/W
	(θ_{JC})ST / SN / UA / SP / SQ	223/390/148/116/410	℃/W
Package Power Dissipation, (P_D)ST/SN/UA/SP/SQ		400/230/606/200/230	mW

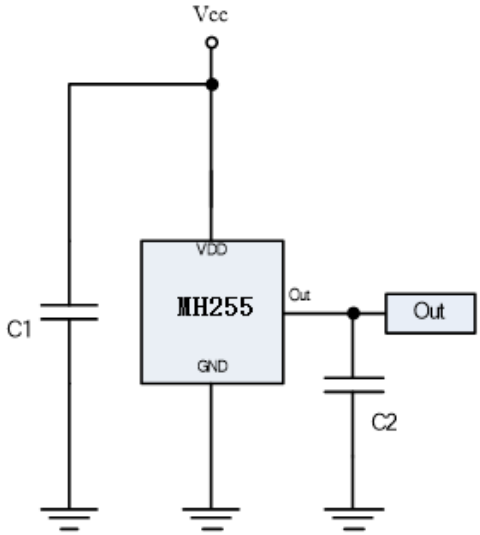
Note: *Exceeding the absolute maximum ratings may cause permanent damage. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.*

Electrical Specifications

DC Operating Parameters： Ta=25℃, V_{DD}=1.8V

Parameters		Test Conditions	Min	Typ	Max	Units
Supply Voltage, (V_{DD})		Operating	1.7		5.5	V
Supply Current, (I_{DD})		Awake State		1.4	3	mA
		Sleep State		3.6	7	μA
		Average		5		μA
Output Leakage Current, (I_{off})		Output off			1	uA
Output High Voltage, (V_{OH})		I_{OUT}=0.5mA(Source)	**V_{DD}-0.2**			V
Output Low Voltage, (V_{OL})		I_{OUT}=0.5mA(Sink)			0.2	V
Awake mode time, (Taw)		Operating		40	80	uS
Sleep mode time, (T_{SL})		Operating		40	80	mS
Duty Cycle, (D,C)				0.1		%
Electro-Static Discharge		HBM	4			KV
Operate Point	($B_{OP}S$)	S pole to branded side, B > BOP, Vout On	20	30	40	Gauss
	($B_{OP}N$)	N pole to branded side, B > BOP, Vout On	-40	-30	-20	Gauss
Release Point	($B_{RP}S$)	S pole to branded side, B < BRP, Vout Off	10	20	30	Gauss
	($B_{RP}N$)	N pole to branded side, B < BRP, Vout Off	-30	-20	-10	Gauss
Hysteresis, (BHYS)		$\lvert B_{OP}X - B_{RP}X \rvert$		10		Gauss

Typical Application circuit

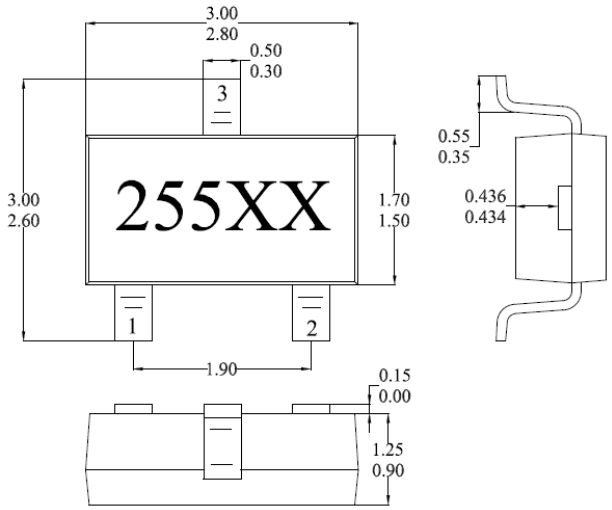


C1：10nF

Sensor Location, package dimension and marking

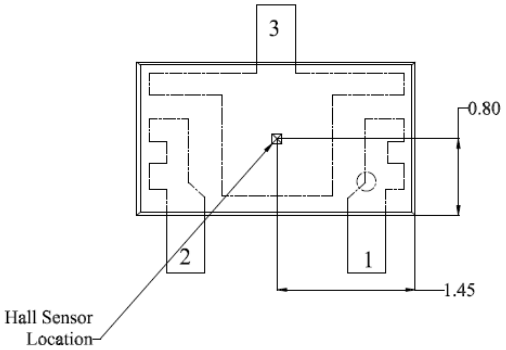
SO Package (SOT-23)

(Top View)

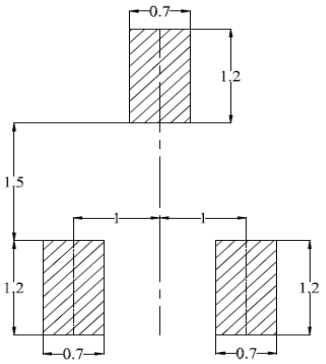


Hall Plate Chip Location

(Bottom view)



(For reference only)Land Pattern

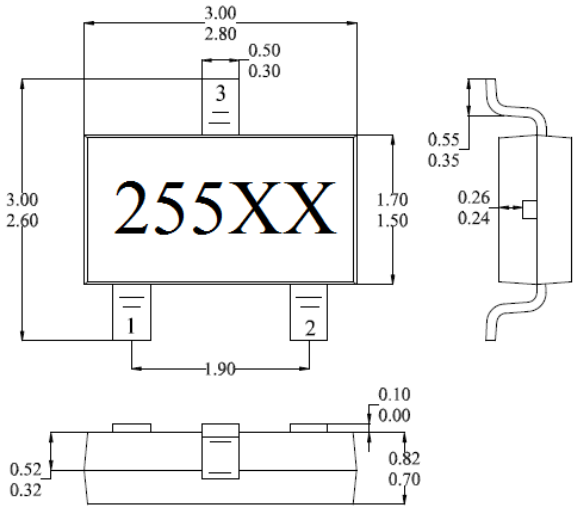


NOTES:

1. PINOUT (See Top View at left :)
   Pin 1 V_{DD}；Pin 2 Output；Pin 3 GND
2. Controlling dimension: mm
3. Lead thickness after solder plating will be 0.254mm maximum
4. XX: Date Code, Refer to DC table

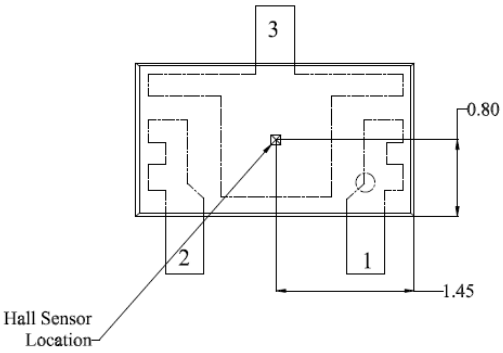
ST Package (TSOT-23)

(Top View)

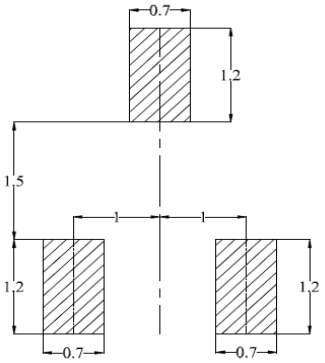


Hall Plate Chip Location

(Bottom view)



(For reference only) Land Pattern

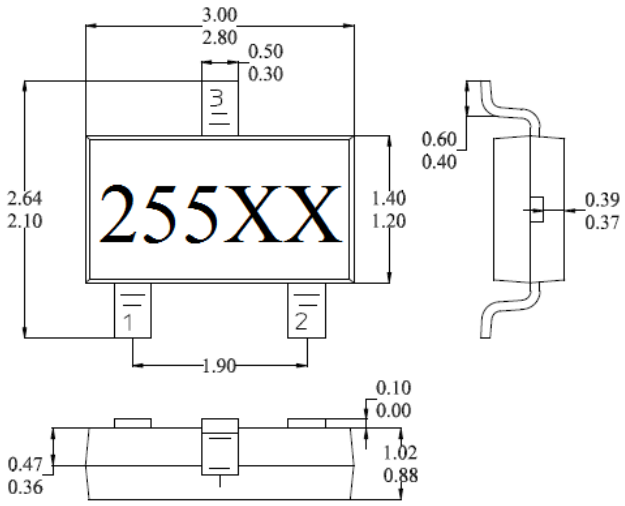


NOTES:

1. PINOUT (See Top View at left :)
   Pin 1 V_{DD}； Pin 2 Output； Pin 3 GND
2. Controlling dimension: mm
3. Lead thickness after solder plating will be 0.254mm maximum
4. XX: Date Code, Refer to DC table

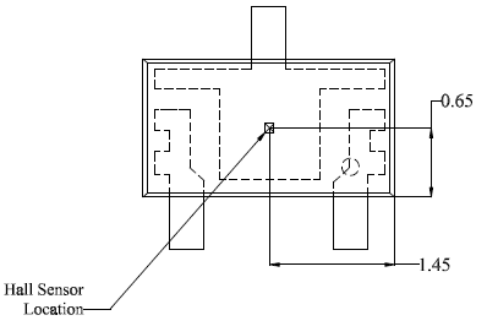
SP Package (PSOT-23)

(Top View)

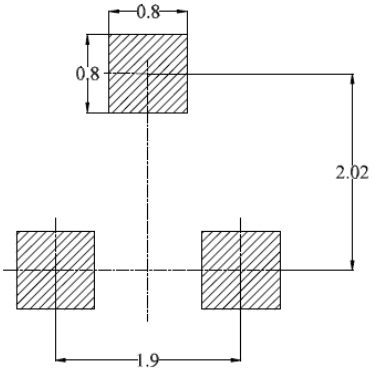


Hall Plate Chip Location

(Bottom view)



(For Reference only) Land pattern

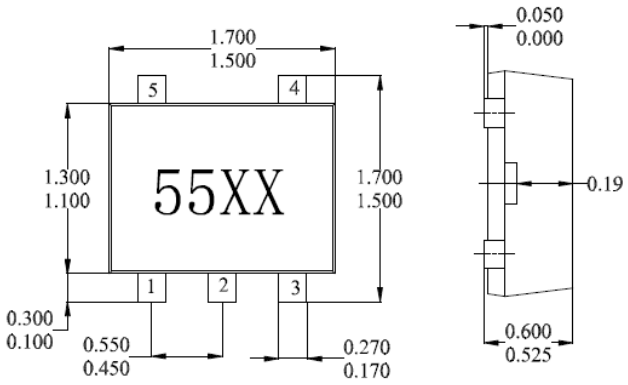


NOTES:

1. PINOUT (See Top View at left :)
   Pin 1 V_{DD}； Pin 2 Output； Pin 3 GND
2. Controlling dimension: mm
3. Lead thickness after solder plating will be 0.254mm maximum
4. XX: Date Code, Refer to DC table

SN Package (SOT-553)

(Top View)

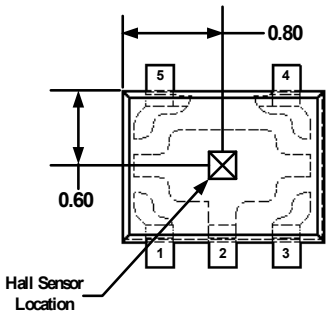


NOTES:

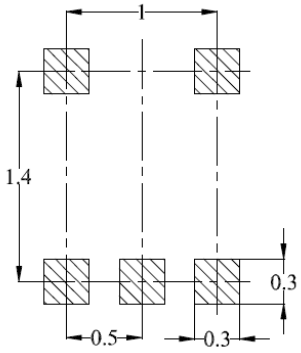
1. PINOUT (See Top View at left:)
   - Pin 1 NC
   - Pin 2 GND
   - Pin 3 NC
   - Pin 4 VDD
   - Pin 5 Out
2. Controlling dimension: mm;
3. XX: Date Code, Refer to DC table

Hall Plate Chip Location

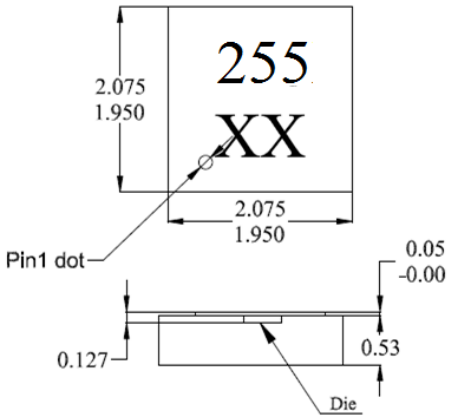
(Bottom view)

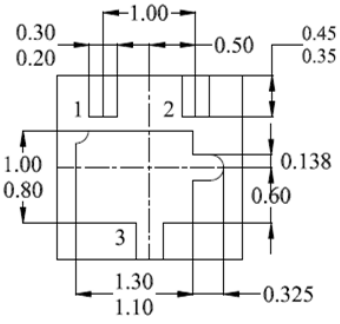


(For reference only)Land Pattern



SQ Package (SQ2020-3）





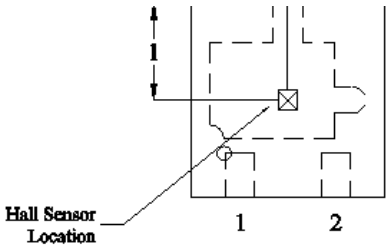
Bottom View

NOTES:

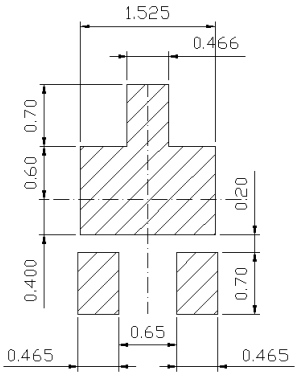
1. PINOUT (See Top View at left)
   - Pin 1 VDD
   - Pin 2 Output
   - Pin 3 GND
2. Controlling dimension: mm;
3. Chip rubbing will be 10mil maximum;
4. Chip must be in PKG. center.
5. XX: Date Code, Refer to DC table

Hall Plate Chip Location

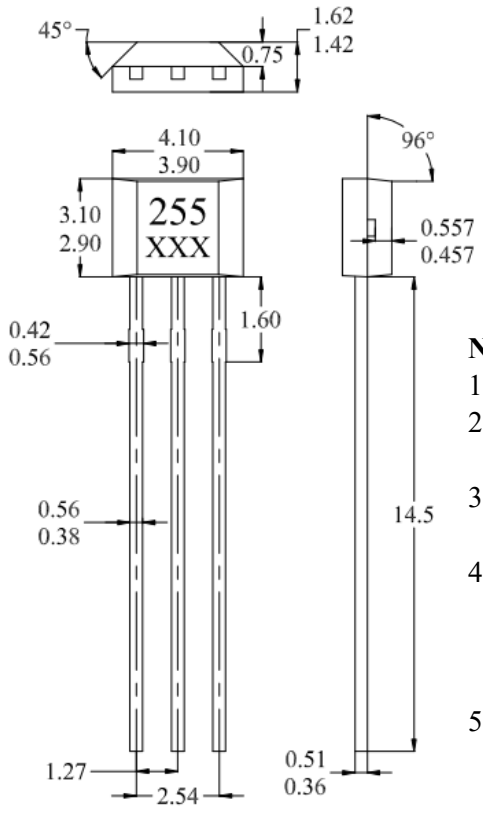
(Top view)



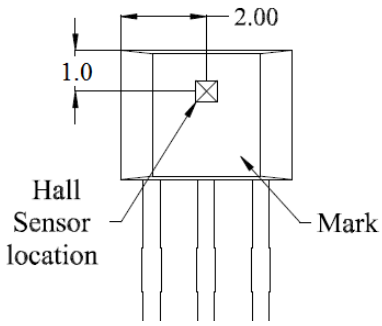
(For reference only)Land Pattern



UA Package (TO-92S)



Hall Chip location



NOTES:

1. Controlling dimension: mm
2. Leads must be free of flash and plating voids
3. Do not bend leads within 1 mm of lead to package interface.
4. PINOUT:
   Pin 1 VDD
   Pin 2 GND
   Pin 3 Output
5. XXX; 1st X=Year;
   2nd and 3rd XX=Week

Output Pin Assignment

(Top view)