MH490 is a monolithic programmable Hall sensor IC featuring the planar Hall technology, which is sensitive to the flux density applied orthogonally to the IC surface. The sensor provides an output signal proportional to the applied magnetic flux density and is preferably suited for current measurement.

The transfer characteristic of MH490 is factory trimmed over temperature,and is programmable (offset, gain) during end-of-line customer calibration. The linear analog output is designed for applications where a very fast response is required, such as inverter applications.

In a typical application, the sensor is used in combination with a soft ferromagnetic core. This core is recommended to be laminated for high bandwidth applications. The Hall IC is placed in a small air gap and the current conductor is passed through the inner part of the ferromagnetic core.

The core concentrates and amplifies the magnetic flux on the Hall sensor IC, which generates an output voltage proportional to the current flowing in the conductor.

Broken ground wire detection, clamps, power-on reset, and under/overvoltage detection provide the required diagnostics for safety-critical automotive applications.

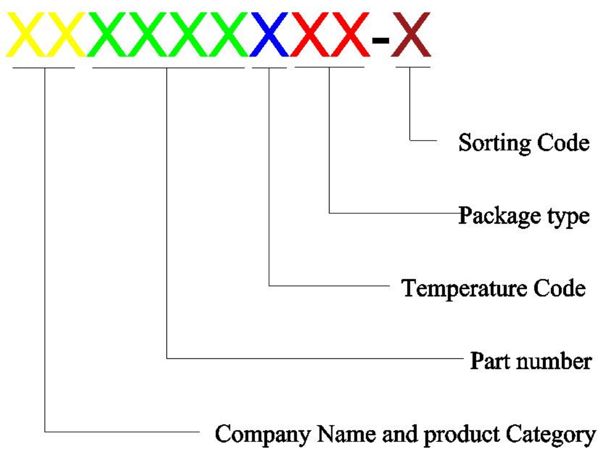
## *Features and Benefits*

- End-of-line programmable sensor
- User-selectable internal or external reference voltage
- User-selectable ratiometry of QVO
- User-selectable ratiometry of Sensitivity
- Measurement range from ±0.9 to ±25mV/G
- Wideband sensing: DC to 240KHz
- Very short response time ~2μs
- RoHS compliant
- TO94(4-pin) package
- MSL-1
- Automotive Grade AECQ100 with diagnostics for safety-critical

## *Applications*

- High Voltage Traction Motor Inverter
- 48V Boost Recuperation Inverter
- DC/DC Converter
- BLDC motor current monitoring
- Smart Fuse Overcurrent Detection

## *Ordering Information*




**Company Name and Product Category**

**MH:MST Hall Effect/MP:MST Power IC**

**Part number**

**181,182,183,184,185,248,249,276,477,381,381F,381R,382…..**

**If part # is just 3 digits, the forth digit will be omitted.**

**Temperature range**

**E: 85 ℃, I: 105 ℃, K: 125 ℃, L: 150 ℃**

**Package type**

**UA:TO-92S, VK:TO-94(4pin), VF:TO-92S(5pin),**

**SO:SOT-23,SQ:QFN-3,ST:TSOT-23,SN:SOT-553,**

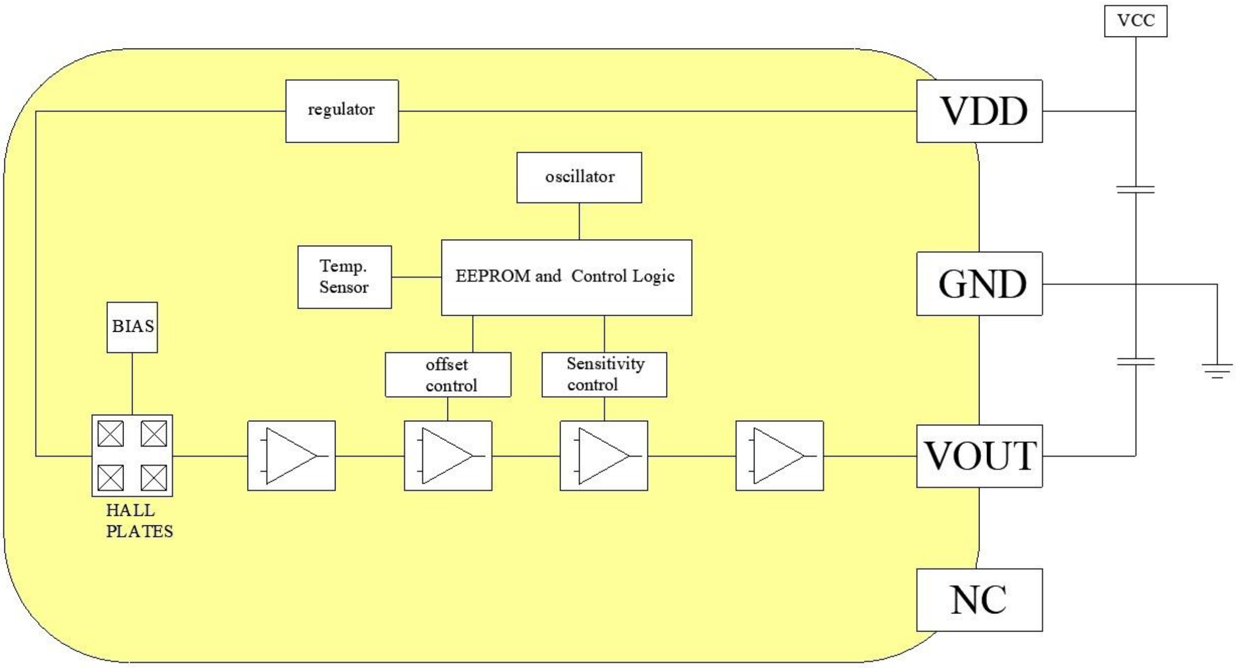
**SF:SOT-89(5pin),SS:TSOT-26,SD:DFN-6**

**Sorting**

**α, β ,Blank…..**

| Part No. | Temperature Suffix | Package Type |
|---|---|---|
| MH490KVK | K (-40℃ to + 125℃) | VK (To-94-4pin) |
| MH490MKVK | K (-40℃ to + 125℃) | VK (To-94-4pin) |

## *Functional Diagram*



## *Absolute Maximum Ratings* *At (Ta=25℃)*

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Positive Supply Voltage (overvoltage) | $V_{DD}$ | 10.5 | V |
| Reverse Voltage | $VS_{REV}$ | -0.3 | V |
| Positive Output Voltage | $V_{OUT}$ | 5.5 | V |
| Output Sink Current | $I_{Sink}$ | -40 | mA |
| Output Source Current | $I_{Source}$ | 60 | mA |
| Reverse Output Voltage | $VO_{REV}$ | -0.3 | V |
| Reverse Output Current | $IO_{REV}$ | -50 | mA |
| Operating Ambient Temperature Range | $T_A$ | -40 to +125 | °C |
| Storage Temperature Range | $T_S$ | -40 to +150 | °C |
| ESD – Human Body Model | $ESD_{HBM}$ | 8 | KV |
| Maximum Number of EEPROM Write Cycles | $EEPROM_{W(max)}$ | 1000 | cycle |

***Note***:*Exceeding the absolute maximum ratings may cause permanent damage. Exposure to absolute maximum - rated conditions for extended periods of time may affect device reliability.*

## *General Electrical Specifications*

*Operating Parameters $T_A$ = -40 to 125°C, $V_{DD}$ = 5V±10%, unless otherwise specified.*

| Parameter | Symbol | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Nominal Supply Voltage | $V_{DD}$ | | 4.5 | 5 | 5.5 | V |
| Supply Current | $I_{DD}$ | No OUT load | | 13 | 18 | mA |
| Power-On Reset Voltage | $V_{POR(H)}$ | $T_A$ = 25°C, $V_{DD}$ rising | 2.82 | 3.0 | 3.25 | V |
| | $V_{POR(L)}$ | $T_A$ = 25°C, $V_{DD}$ falling | 2.58 | 2.8 | 3.06 | V |
| Power-On Reset Hysteresis | $V_{POR(HYS)}$ | $T_A$ = 25°C | 158 | 200 | 190 | mV |
| Power-On Delay Time | $t_{PO}$ | $T_A$ = 25°C, $C_{BYPASS}$ = 104, CL = 1 nF | | | 1 | ms |
| Overvoltage Detection | $V_{OVD(EN)}$ | $T_A$ = 25°C | 6.35 | 6.50 | 6.70 | V |
| | $V_{OVD(DIS)}$ | $T_A$ = 25°C | 5.85 | 6.00 | 6.20 | V |
| OVD Hysteresis | $V_{OVD(HYS)}$ | $T_A$= 25°C | | 0.50 | | mV |
| Undervoltage Detection | $V_{UVD(H)}$ | $T_A$ = 25°C | 4.10 | 4.20 | 4.35 | V |
| | $V_{UVD(L)}$ | $T_A$ = 25°C | 3.70 | 3.80 | 3.95 | V |
| UVD Hysteresis | $V_{UVD(HYS)}$ | $T_A$ = 25°C | | 400 | | mV |
| OVD and UVD Enable/Disable Delay Time | $t_{VD(EN)}$ | $T_A$ = 25°C | 7 | 14 | 21 | us |
| | $t_{VD(DIS)}$ | $T_A$ = 25°C | 7 | 14 | 21 | us |
| Linear Output Range | $VO_{LIN}$ | pull-down ≥ 10 kΩ | 10 | | 90 | %Vdd |

## *Analog output specification*

Accuracy specifications

*Operating Parameters TA = -40 to 125°C, VDD = 5V±10%, unless otherwise specified.*

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Output Impedance | $R_{OUT}$ | Normal Operation | | 8 | | Ω |
| Output Capacitive Load | $C_L$ | | | 10 | 68 | nF |
| Output Resistive Load | $R_L$ | | 4.7 | 10 | | KΩ |
| VOUT pin sink/source current | | $V_{OUT}$ shorted to $V_{DD}$ | | | -20 | mA |
| | | $V_{OUT}$ shorted to $G_{ND}$ | 28 | | | mA |
| Output Voltage Clamp | $V_{CLP(HIGH)}$ | $T_A$ = 25°C, $R_L$ = 10 KΩ to GND, Bias = 400 G | | $V_{DD}$-( $V_{DD}$*0.06) | $V_{DD}$-0.25 | V |
| | $V_{CLP(LOW)}$ | $T_A$ = 25°C, $R_L$ = 10 KΩ to $V_{DD}$, Bias = 400 G | 0.25 | $V_{DD}$*0.06 | | V |
| Output Voltage with Broken GND/VDD | $V_{BRK\_DN}$ | $T_A$ = 25°C, $R_L$ = 10 KΩ to GND, Pin 3 = NC | | 100 | 200 | mV |
| | $V_{BRK\_UP}$ | $T_A$ = 25°C, RL = 10 KΩ to $V_{DD}$ (5V), Pin 3 = NC | 4.8 | 4.9 | 5 | V |
| $V_{OQ}$ Ratiometry | $\Delta^R V$ | $V_{DD}$ = 5V±5%, $V_{OQ}$ = 50%$V_{DD}$ | | ±0.24 | ±0.4 | %$V_{OQ}$ |
| RMS Output Noise(high-gain) | $N_{RMS-HG}$ | Values for S=12.5mV/G, 1KHz-100KHz | | 7 | | mVRMS |
| Temperature coefficient variation of Sensitivity | $\delta_{TCVO}$ | Over full range of BM and $T_A$, calibrated IC, without $TC_{OF}$ | -200 | | 200 | ppm/°C |
| Offset Temperature characteristic | $TC_{VOF}$ | BM = 0G, S=12.5mV/G, $V_{OUT}$ – $V_{DD}$/2 | -0.120 | | 0.120 | mV/°C |
| Average Fine Sensitivity Programming Step Size | $Step_{SENS}$ | S=12.5mV/G, TA = 25°C | | 1.5 | | µV/G |

***Note****:The accuracy specifications are defined for the factory calibrated sensitivity. The achievable accuracy is dependent on the user's end-of-line calibration.*

### Timing specifications

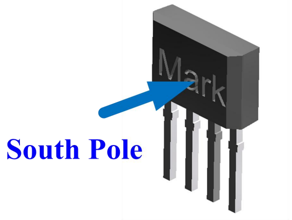
*Operating Parameters $T_A$ = -40 to 125°C, $V_{DD}$ = 5V±10%, unless otherwise specified.*

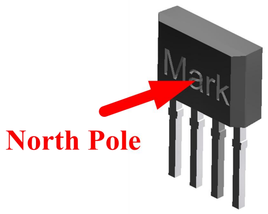
| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Response Time | tRESP | $T_A$ = 25 °C, $C_L$=1nf, Magnetic field step of 400G, Sens=2mV/G, Measured 90% input to 90% output. | | 2 | | µs |
| Frequency bandwidth | BW | -3 dB, TA = 25 °C | | 240 | | kHz |

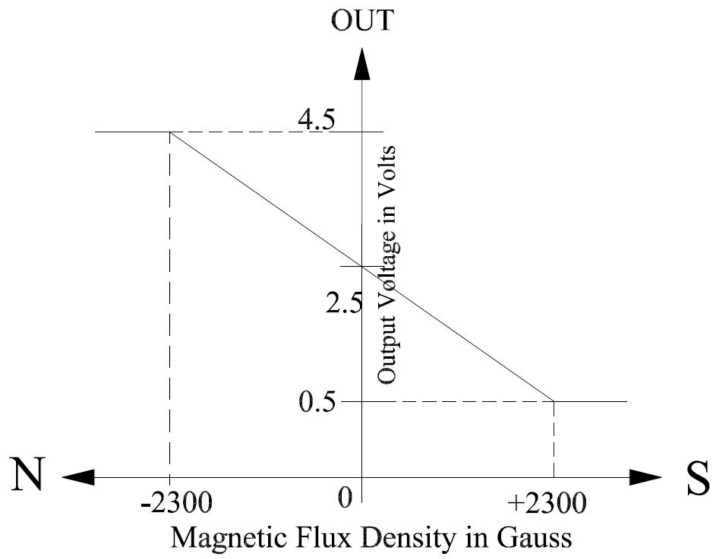
## *Magnetic specification*

*Operating Parameters $T_A$ = -40 to 125°C, $V_{DD}$ = 5V±10%, unless otherwise specified.*

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Operational Magnetic Field Range | BOP | | ±100 | ±1000 | ±2300 | G |
| Programmable Sensitivity | S | | 0.9 | 2 | 25 | mV/G |
| Linearity Error (Magnetic) | NL | $V_{OUT}$ in [10%$V_{DD}$, 90%$V_{DD}$], $T_A$ = 25°C, $R_L \geq 10$ kΩ | | | ±0.25 | %FS |



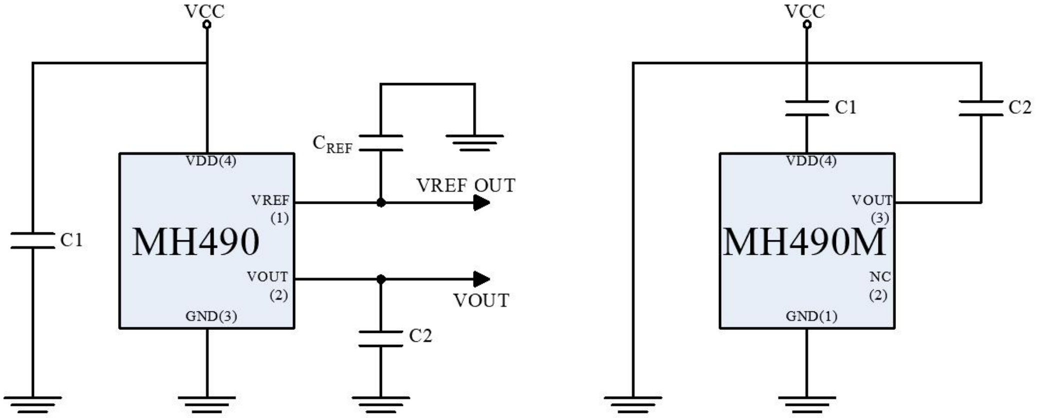



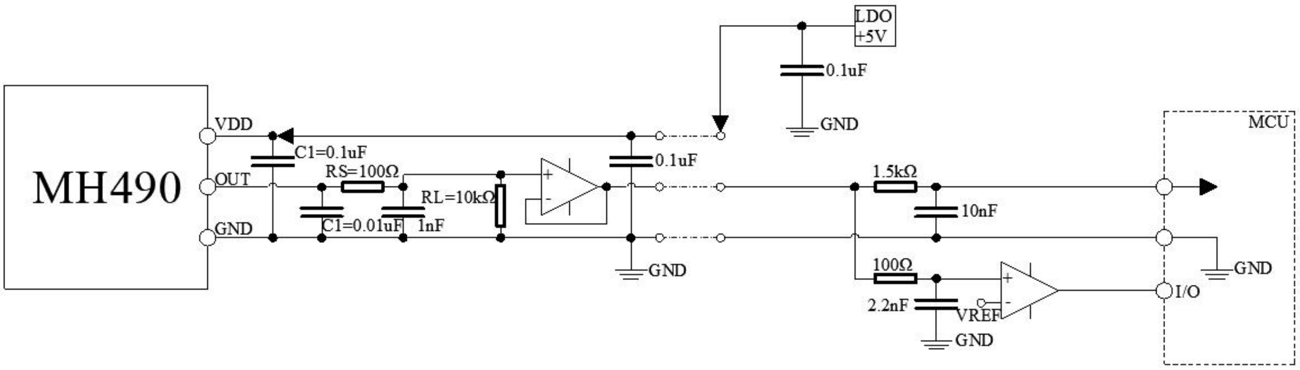

## *Programmable Items*

| Parameter | Bits | Factory Setting | Comment |
|---|---|---|---|
| QVO[4:0] | 5 | trimmed | Quiescent output level (0 Gauss) adjustment |
| RG[4:0] | 5 | trimmed | Rough gain adjustment |
| FG[7:0] | 8 | trimmed | Fine gain adjustment |
| POL | 1 | 0 | 0: default polarity as described in section 11 (figure 4) |
| | | | 1: opposite polarity |
| ID[19:0] | 20 | | CUSTOMER ID |

## *Recommended Application Diagram*




## *Application Circuit for Harsh and Noisy Environment*




For proper operation a 100nF or bigger bypass capacitor C1 should be placed as close as possible to the VDD and GND pins, and a bypass capacitor C2 of 1nF to 10nF can be placed on the output of MH490.

## *ESD Precautions*

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).
Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

## *Under- and overvoltage detection (UVD, OVD)*

Under- and overvoltage detection is implemented to prevent the device from operating outside the required supply voltage range. A fault condition is detected if the supply voltage is below or above the limits. The undervoltage detection is kept in reset (undervoltage detected) during the start-up of the device and is released by the digital as soon as the digital finished the EEPROM reading. The overvoltage detection can be enabled/disabled by the EEPROM.

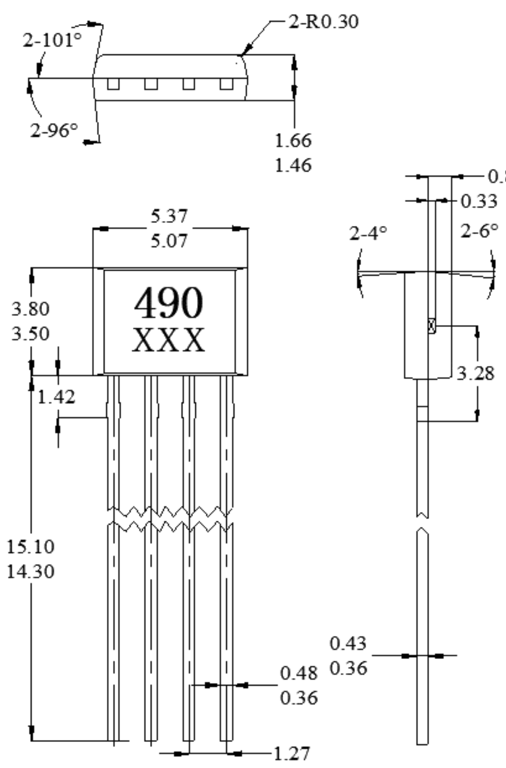
The outputs of the UVD and OVD are used to force the VREF and VOUT to predefined states incase of a detected fault.

| Condition | Description | VREF output | VOUT output |
|---|---|---|---|
| UVD | During device startup and UVD detected | Forced to GND | Floating (Hi-Z) |
| OVD | OVD detected (only when EN_OVD = 1) | VREF | Floating (Hi-Z) |

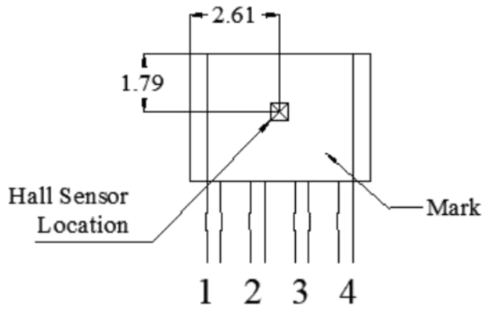
The VREF output is forced to GND during startup of the device and at an undervoltage condition. The VREF output stays in normal operation at an overvoltage condition.
The $V_{OUT}$ output is forced to Hi-Z mode in both the UVD and OVD condition. These fault conditions can be detected by a connected controller in case a pull-up or pull-down resistor at $V_{OUT}$ is used ($V_{OUT} = V_{CC}$ or $V_{OUT}$ = GND).

## *MH490 Sensor Location, package dimension and marking*

**VK Package (To-94-4pin)**



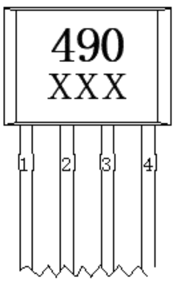

**Hall Chip location**




**NOTES:**
1.Controlling dimension: mm
2.Leads must be free of flash and plating voids
3.Do not bend leads within 1 mm of lead to package interface.
4.PINOUT:

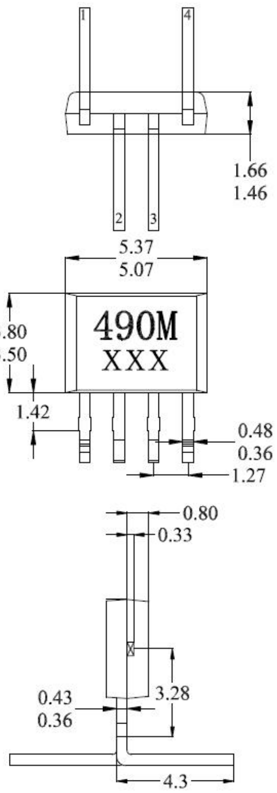
| | |
|---|---|
| Pin 1 | VREF |
| Pin 2 | VOUT |
| Pin 3 | GND |
| Pin 4 | VCC |

**Output Pin Assignment**

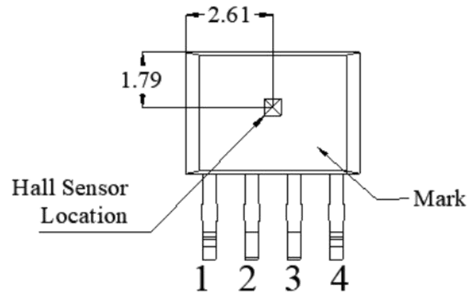


## *MH490M Sensor Location, package dimension and marking*

**VK Package (To-94-4pin)**




**Hall Chip location**




**NOTES:**

1.Controlling dimension: mm
2.Leads must be free of flash
and plating voids
3.Do not bend leads within 1 mm
of lead to package interface.
4.PINOUT:

Pin 1 GND
Pin 2 GND
Pin 3 VOUT
Pin 4 VDD

**Output Pin Assignment**